LISTING OF THE CLAIMS

Claims 1-41 are pending. Claims 1-2, 6, 11-13, 19-21, 27-29, 31-33 and 35-36 have been amended for clarity, without acquiescence or prejudice to pursue in a related application. A complete listing of the current pending claims is provided below and supersedes all previous claims listing(s). No new matter has been added.

1. (Currently Amended) A computer-implemented method for determining a worst-case transition comprising:

determining at least a plurality of different arrival times and a plurality of different slews from a plurality of timing events propagated to an input of a gate based at least in part upon a timing model of the gate;

selecting by a processor one of the plurality of timing events propagated to the input of the gate as a worst case timing event based at least in part upon ~~at least~~ a load data ~~combination~~ of the gate~~'s characteristics~~, an arrival time in the plurality of different arrival times and a slew in the plurality of different slews of the plurality of timing events; and

storing information related to the worst-case timing event in a computer readable medium.

2. (Currently Amended) The method of claim 1, further comprising:

determining a plurality of gate delays for a plurality of input signals based at least in part upon the timing model of the gate.

3. (Previously Presented) The method of claim 2, wherein selecting a worst-case input timing event further comprises:

selecting a worst delay based on the gate delays.

4. (Previously Presented) The method of claim 1, wherein the timing model comprises:

$T_o = T_i + D_g$,

$D_g = F(S_i, C)$,

$S_o = Q(S_i, C)$;

where T_o is an output time, T_i is an input time, D_g is a gate delay, S_i is an input slew, C is a capacitive load of the gate, and S_o is an output slew, wherein the delay D_g of the gate depends, at least in part, on the slew of the input transition and the capacitive load at the output of the gate.

5. (Original) The method of claim 1, wherein the timing model is a timing library format (TLF) model.

6. (Currently Amended) An apparatus for determining a worst case transition comprising:

means for determining at least a plurality of arrival times and a plurality of slews for a plurality of input signals propagated to an input of a gate based at least in part upon a timing model of the gate; [[and]]

[[means]] a processor for selecting one of the plurality of input signals propagated to the input of the gate as a worst delay input signal based at least in part upon ~~at least~~ a load data ~~combination~~ of the gate~~'s characteristics~~, an arrival time in the plurality of arrival times and a slew in the plurality of slews of the input signals; and

a computer readable medium for storing information related to the worst delay input signal.

7. (Original) The apparatus of claim 6, further comprising:

means for determining a plurality of gate delays for a plurality of input signals based on the timing model of the gate.

8. (Previously Presented) The apparatus of claim 7, wherein said means for selecting a worst-case input timing event further comprises:

means for selecting a worst delay based on the gate delays.

9. (Previously Presented) The apparatus of claim 6, wherein the timing model comprises:

$$T_o = T_i + D_g,$$

$$D_g = F(S_i, C),$$

$$S_o = Q(S_i, C);$$

where T_o is an output time, T_i is an input time, D_g is a gate delay, S_i is an input slew, C is a capacitive load of the gate, and S_o is an output slew, wherein the delay D_g of the gate depends, at least in part, on the slew of the input transition and the capacitive load at the output of the gate.

10. (Original) The apparatus of claim 6, wherein the timing model is a timing library format (TLF) model.

11. (Currently Amended) A computer readable medium storing a computer program comprising instructions which, when executed by a processing system, cause the system to perform a method for determining a worst case transition, the method comprising:

determining at least a plurality of different arrival times and a plurality of different slews from a plurality of timing events propagated to an input of a gate based at least in part upon a timing model of the gate;

selecting one of the plurality of timing events propagated to the input of the gate as a worst case timing event based at least in part upon ~~at least~~ a load data ~~combination~~ of the gate~~'s characteristics~~, an arrival time in the plurality of different arrival times and a slew in the plurality of different slews of the plurality of timing events; and

storing information related to the worst-case timing event.

12. (Currently Amended) The medium of claim 11, further comprising instructions, which, when executed by the processing system, cause the system to perform the method for determining a worst case transition, the method further comprising:

determining a plurality of gate delays for a plurality of input signals based at least in part upon the timing model of the gate.

13. (Currently Amended) The medium of claim 12, further comprising instructions, which, when executed by the processing system, cause the system to perform the method for determining a worst case transition, wherein selecting a worst-case input timing event further comprises:

selecting a worst delay based at least in part upon the gate delays.

14. (Previously Presented) The medium of claim 11, wherein the timing model comprises:

$$T_o = T_i + D_g,$$

$$D_g = F(S_i, C),$$

$$S_o = Q(S_i, C);$$

where T_o is an output time, T_i is an input time, D_g is a gate delay, S_i is an input slew, C is a capacitive load of the gate, and S_o is an output slew, wherein the delay D_g of the gate depends, at least in part, on the slew of the input transition and the capacitive load at the output of the gate.

15. (Original) The medium of claim 11, wherein the timing model is a timing library format (TLF) model.

16. (Previously Presented) The method of claim 1, wherein the slews of the output timing events include slew rates of the output timing events, which is determined by an amount of time for a waveform to transition from a first voltage level to a second voltage level.

17. (Previously Presented) The apparatus of claim 6, wherein the output slews of the output timing events include output slew rates of the output timing events, which is determined by an amount of time for a waveform to transition from a first voltage level to a second voltage level.

18. (Previously Presented) The medium of claim 11, wherein the output slews of the output timing events include slew rates of the output timing events, which is determined by an amount of time for a waveform to transition from a first voltage level to a second voltage level.

19. (Currently Amended) A computer-implemented method for determining a worst-case timing event comprising:

determining a plurality of arrival times and a plurality of slew rates from a plurality of input timing events propagated to an input of a gate based at least in part upon a timing model and a capacitive load of the gate;

selecting by a processor one of the plurality of input timing events propagated to the input of the gate as a worst delay input signal based at least in part upon a load data of the gate~~'s characteristics~~, an arrival time in the plurality of different arrival times and a slew rate in the plurality of different slews rates determined on the output of the gate; and

storing information related to the worst-case input timing event in a computer readable medium.

20. (Currently Amended) The method of claim 19, further comprising:

determining a plurality of gate delays for a plurality of input signals based at least in part upon the timing model of the gate.

21. (Currently Amended) The method of claim 20, wherein selecting a worst-case input timing event further comprises:

selecting a worst delay based at least in part upon the gate delays.

22. (Previously Presented) The method of claim 19, wherein the timing model comprises:

$$T_o = T_i + D_g,$$

$$D_g = F(S_i, C),$$

$$S_o = Q(S_i, C);$$

where T_o is an output time, T_i is an input time, D_g is a gate delay, S_i is an input slew, C is a capacitive load of the gate, and S_o is an output slew, wherein the delay D_g of the gate depends, at least in part, on the slew of the input transition and the capacitive load at the output of the gate.

23. (Previously Presented) The method of claim 19, wherein the timing model is a timing library format (TLF) model.

24. (Previously Presented) The method of claim 1, wherein the different arrival times comprise the arrival times of the timing events at each input of the gate.

25. (Previously Presented) The method of claim 24, wherein the different arrival times of the timing events at each input of the gate comprises the input times of the timing events.

26. (Previously Presented) The method of claim 1, wherein the different slews comprise transition times of the timing events through the gate.

27. (Currently Amended) The method of claim 26, wherein the transition times of the timing events through the gate are based at least in part upon characteristics of the gate.

28. (Currently Amended) The method of claim 26, wherein a duration of the transition times of the timing events through the gate is based at least in part upon characteristics of the gate.

29. (Currently Amended) A computer-implemented method for determining a worst-case transition comprising:

identifying a plurality of timing events propagated to an input of a gate having different arrival times at an input of the gate;

determining different slews from the plurality of the timing events based at least in part upon a timing model of the gate;

selecting by a processor one of the plurality of timing events propagated to the input of the gate as a worst case timing event based at least in part upon a load data ~~combination~~ of the gate~~'s characteristics~~, an arrival time in the plurality of different arrival times and a slew in the plurality of different slews of the plurality of timing events; and

storing information related to the worst-case timing event in a computer readable medium.

30. (Previously Presented) The method of claim 29, wherein the slews comprise transition times of the timing events through the gate.

31. (Currently Amended) The method of claim 30, wherein the transition times of the timing events through the gate are based at least in part upon characteristics of the gate.

32. (Currently Amended) The method of claim 30, wherein a duration of the transition times of the timing events through the gate is based at least in part upon characteristics of the gate.

33. (Currently Amended) A computer-implemented method for determining a worst-case transition comprising:

identifying a plurality of timing events having different propagation delays;

determining different arrival times and different slews of the timing events propagated to an input of a gate based at least in part upon a timing model of the gate;

selecting by a processor one of the plurality of timing events propagated to the input of the gate as a worst case timing event based at least in part upon ~~at least a~~ load data ~~combination~~ of the gate~~'s characteristics~~, an arrival time in the plurality of different arrival times and a slew in the plurality of different slews of the timing events; and

storing information related to the worst-case timing event in a computer readable medium.

34. (Previously Presented) The method of claim 33, wherein the slews comprise transition times of the timing events through the gate.

35. (Currently Amended) The method of claim 34, wherein the transition times of the timing events through the gate are based at least in part upon characteristics of the gate.

36. (Currently Amended) The method of claim 34, wherein a duration of the transition times of the timing events through the gate is based at least in part upon characteristics of the gate.

37. (Previously Presented) The method of claim 1, 19, 29 or 33, wherein information related to the worst-case timing event is stored in a memory device.

38. (Previously Presented) The apparatus of claim 6, further comprising a means for storing information related to the worst delay input signal.

39. (Previously Presented) The apparatus of claim 38, wherein the means for storing information related to the worst delay input signal comprises a memory device.

40. (Previously Presented) The medium of claim 11, wherein information related to the worst delay input signal is stored on a memory device.

41. (Previously Presented) The method of claim 19, wherein information related to the worst-case input timing event is stored on a memory device.